RESEARCH ARTICLE OPEN ACCESS

Analysis of Conventional Sram 6t at Low Power and High Perfomamce 32nm Technologies

Loveneet Mishra
MTECH (Advanced electronics and communication with specialization in Vlsi Design) Jss Academy Of Technical Education, Noida

Abstract
Here we analysis and compare the conventional SRAM 6t at two different nano-scale technologies. First is low power 32nm PTM technology and second is high performance 32nm PTM technology. At low power 32nm PTM technologies power dissipation is significantly reduces at reducing power supply but both read and write delay increases drastically. In other side, at high performance 32nm PTM technologies power dissipation reduces at reducing the power supply, and read delay increase moderate but write delay reduces gives the high performance and low power SRAM, all the simulation is done in Tanner Tool.
Keywords-- SRAM 6T, LP-32PTM, HP-32PTM

I. INTRODUCTION

High performance and Low power SRAMs have become a critical component in field of VLSI chips design. This is truly applicable for microprocessors, where the on-chip cache sizes are rapidly growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory to enhance the performance. Simultaneously, power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the significantly growth of battery operated appliances. This paper explores the design of SRAMs, focusing on optimizing delay and power. While power supply scaling remain the biggest drivers of fast low power designs, this paper analysis SRAM 6T cell at nano-scale technologies which can be used in conjunction to scaling to achieve high performance & low power operation.

II. SRAM 6T Cell Design

The schematic diagram of 6T SRAM cell is shown in Figure.1

During read, the WL voltage VWL is raised, and the memory cell discharges either BL (bit line true) or BLB (bit line complement), depending on the stored data on nodes Q and QB. A sense amplifier converts the differential signal to a logic-level output. Then, at the end of the read cycle, the BLs returns to the positive supply rail. During write, VWL is raised and the BLs are forced to either VDD (depending on the data), overpowering the contents of the memory cell. During hold, VWL is held low and the BLs are left floating or driven to VDD.[5]

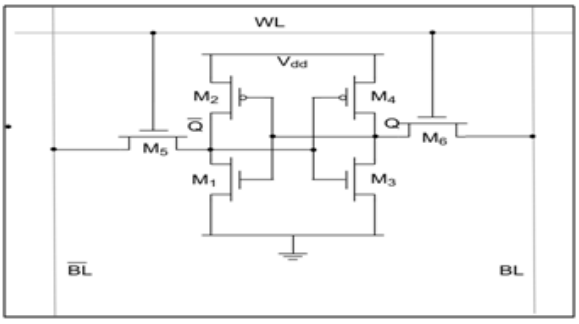

Figure.1. SRAM 6T cell

III. SIMULATION RESULT

Here we use the tanner tool for simulation (T-SPICE, S-EDIT, and W-EDIT). For schematic we use the S-Edit and for net list we go for the T-spice and waveform obtained with the help of W-edit. Technologies used LP-32 PTM technology and HP-32nm PTM technology.[1]

A. SCHEMATIC OF SRAM 6T (S-EDIT)

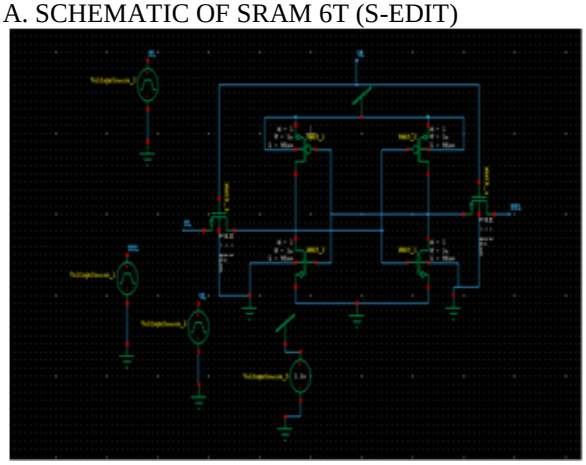
Figure.2. SRAM 6T Schematic

B. OUTPUT WAVEFORM

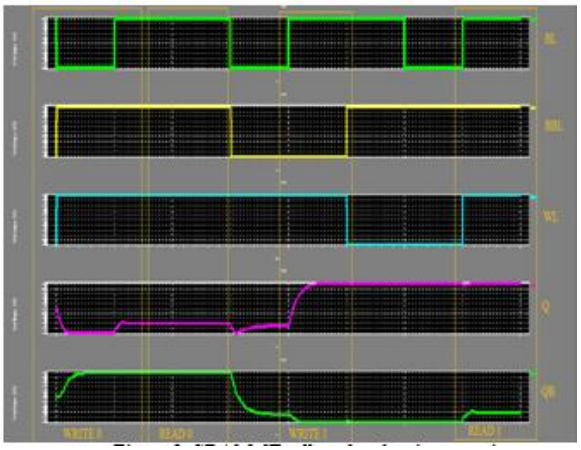

Figure.3. SRAM 6T cell read and write operation

C. AT LOW POWER 32NM PTM TECHNOLOGY

1. TABLE: - VDD Vs READ DELAY

GRAPH

VDD(volts)	Read Delay (seconds)
1.0v	5.9600e-010
0.95v	5.9568e-010
0.90v	5.9897e-010
0.85v	6.0774e-010
0.80v	6.2324e-010
0.75v	6.5390e-010

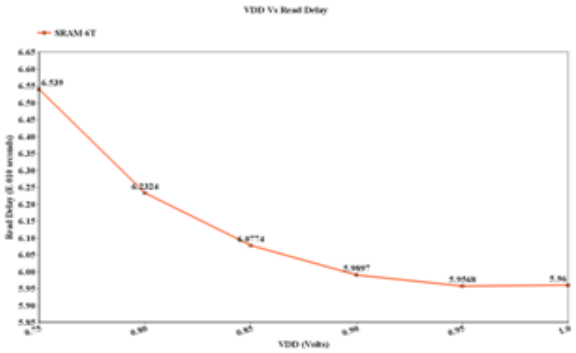

Figure.4. VDD Vs Read Delay

2. TABLE: - VDD Vs AVERAGE POWER DISSIPATION DURING READ OPERATION

VDD (Volts)	Average Power Dissipation (Read) Watts
1.0v	3.888021e-006 watts
0.95v	3.250504e-006 watts
0.90v	2.654298e-006 watts
0.85v	2.105733e-006 watts
0.80v	1.610614e-006 watts
0.75v	1.172662e-006 watts

GRAPH

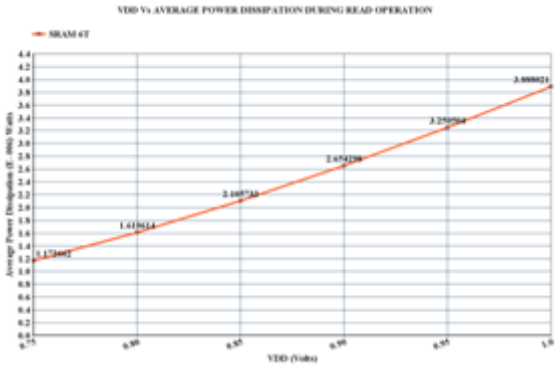

Figure 5.VDD Vs Average Power Dissipation (Read)

3. TABLE: - VDD Vs WRITE DELAY

VDD(volts)	WRITE Delay (seconds)
1.0v	2.1819e-009
0.95v	2.1730e-009
0.90v	2.1715e-009
0.85v	2.1746e-009
0.80v	2.1853e-009
0.75v	2.2081e-009

GRAPH

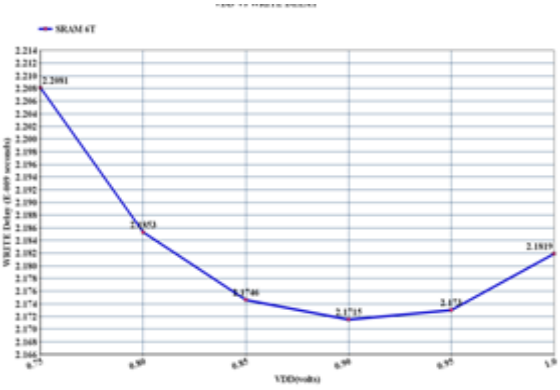

Figure.6. VDD Vs Write Delay

4. TABLE: - VDD Vs AVERAGE POWER DISSIPATION DURING WRITE OPERATION

VDD (Volts)	Average Power Dissipation (WRITE) Watts
1.0v	2.563651e-006 watts
0.95v	2.012949e-006 watts
0.90v	1.559847e-006 watts
0.85v	1.233078e-006 watts
0.80v	9.468235e-007 watts
0.75v	6.948722e-007 watts

GRAPH

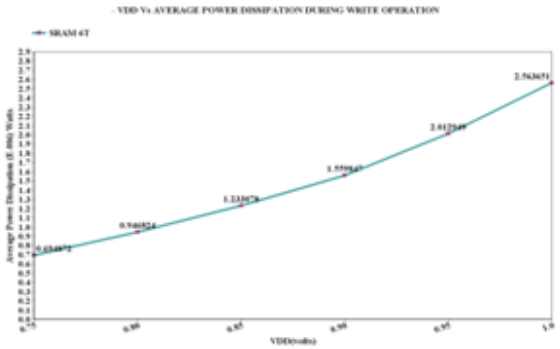

Figure.7. VDD Vs Average Power Dissipation (Write)

D. AT HIGH PERFORMANCE 32NM PTM TECHNOLOGY

1. TABLE: - VDD Vs READ DELAY

VDD(volts)	Read Delay (seconds)
0.90	5.3264e-010
0.85	5.3233e-010
0.80	5.3222e-010
0.75	5.3229e-010
0.70	5.3259e-010
0.65	5.3302e-010

GRAPH

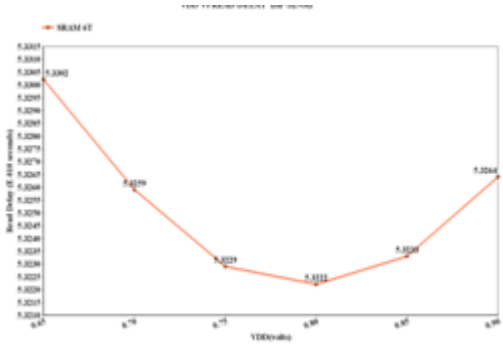

Figure.8. VDD Vs Read Delay

2. TABLE: - VDD Vs AVERAGE POWER DISSIPATION DURING READ OPERATION

VDD (Volts)	Average Power Dissipation (Read) Watts
0.90	9.700527e-006 watts
0.85	7.965107e-006 watts
0.80	6.432747e-006 watts
0.75	5.087699e-006 watts
0.70	3.900864e-006 watts
0.65	2.859051e-006 watts

GRAPH

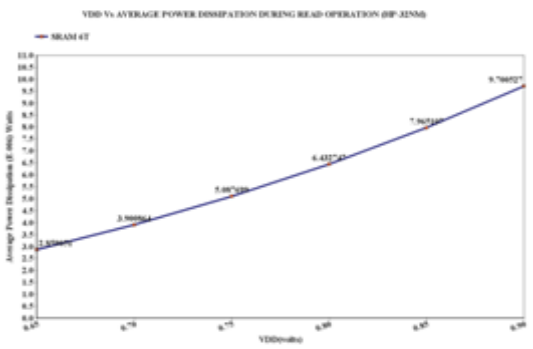

Figure.9. VDD Vs Average Power Dissipation (Read)

3. TABLE: - VDD Vs WRITE DELAY

VDD(volts)	WRITE Delay (seconds)
0.90	2.0563e-009
0.85	2.0537e-009
0.80	2.0514e-009
0.75	2.0494e-009
0.70	2.0457e-009
0.65	2.0378e-009

GRAPH

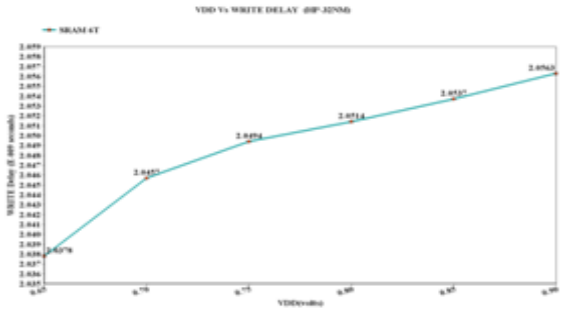

Figure 10. VDD Vs Write Delay

4. TABLE: - VDD Vs AVERAGE POWER DISSIPATION DURING WRITE OPERATION

VDD (Volts)	Average Power Dissipation (WRITE) Watts
0.90	5.270950e-006 watts
0.85	4.476185e-006 watts
0.80	3.661306e-006 watts
0.75	2.791751e-006 watts
0.70	2.161043e-006 watts
0.65	1.558797e-006 watts

GRAPH

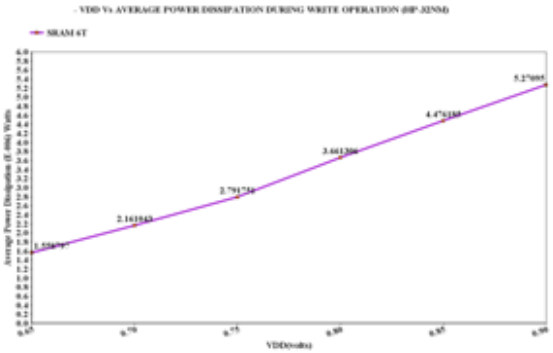

Figure. 11. VDD Vs Average Power Dissipation (Write)

IV. CONCLUSION

From the above observation it is clear that the conventional SRAM 6T gives best performance in High Performance 32 nm PTM technology. In this technology we get low power and high performance.

REFERENCES

[1]. Lab Manuals for T-Spice, S-Edit and L-Edit
[2]. J. M. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall, NJ, 1996.
[3]. Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits" Third edition; Tata McGraw-Hill; New Delhi; (2003)
[4]. VLSI Memory Chip Design By Kiyoo Itoh
[5]. A. Karandikar and K. K. Parhi, Low power SRAM design using hierarchical divided bit-line approach
[6]. J. M. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall, NJ, 1996.